Firm, Insulating and Electrically Conducting Connection of Processed Semiconductor Wafers

The invention relates to a process for connecting processed semiconductor wafers by means of electrically conducting and electrically insulated, structured intermediate connecting layers. A wafer arrangement that can be produced with the process is also involved.

The connecting of processed semiconductor wafers is used in the manufacture of microelectronic and microelectromechanical systems in order to cover specific structures already during the wafer process by a cap. On the one hand, this operation is necessary in order to protect sensitive mechanical structures during subsequent processing steps and/or to implement the actual encapsulation of the individual elements, e.g. optical components, already during wafer bonding and to thus make special structures possible. Customary processes for connecting e.g. system and cover wafers are anodic and direct bonding and bonding by means of low-melting intermediate glass layers (glass frit bonding).

As a rule, the mechanically and/or electrically active elements are located on the system wafer. Whereas the cover layer mostly only serves as a covering protection (cap) and does not have any electrical structures or only has a few electrical structures according to the prior art.

The aforementioned bonding processes have the property that the wafers are not conductingly connected with each other. On the one hand, this is due to the fact that the cover wafer itself is not conducting (anodic bonding). On the other hand, intermediate layers formed during bonding are not conducting (binding oxide during direct bonding, intermediate glass layer during glass frit bonding). When using the encapsulation bonding it is, however, mostly necessary to specifically connect the entire cover and/or structures on the cover in an electrically conducting fashion. An electric connection of the entire cover is partly necessary in order to connect it to a specific potential, e.g. mass.

For the reading of capacitive sensors evaluation electrodes are required on the cover which must have a contact towards the system wafer in order to make a wire bonding during the setting up and connection processes in one plane possible.

To increase the packing density of microsystems it is also advantageous to integrate evaluation circuits on the cover wafer, if they can have an electric contact towards the system wafer. So far, electric wafer-to-wafer contacts have only been known so far from anodic bonding. Here, metallization areas of the wafers to be connected are brought into mechanical contact and are firmly pressed together due to the resultant wafer connection force, cf. KADAR et al., Sensors & Actuators A52 (1996), pages 151 to 155 - Aluminium press-on contacts for glass to silicon anodic bonding.

This process is not completely convincing. On the one hand, the areas of electric contact interfere with the formation of the actual wafer bond connection. On the other hand, there is no material connection in the area of the electric contacts so that their reliability is thus doubtful. The glass frit bonding is considered to be the wafer bonding process for encapsulation purposes that can be used most universally , since it renders very high bonding yields and since, due to the planarizing effect of the molten intermediate glass layer, it balances surface profiles of the wafers to be connected and, thus, makes lateral metallic contact leadthroughs in the bonding interface possible.

The invention is based on the technical object of designing a connection process in such a way that a firm connection that tightly seals with respect to cavities of at least two semiconductor wafers is provided with a simultaneous electric connection of the wafers.

The object is attained with claims 1, 11 or 10 or 20 (as a process and a product).

the combination of conducting and insulating glass structures specifically reaches areas of the cover wafer during glass frit bonding so that they are electrically connected.

The invention is especially suited for microelectromechanical structures which are integrated with structures of the evaluation electronics. Moreover, more than two semiconductor wafers can also be connected with each other as a stack. Then, there are also central areas in this stack, where cover wafer and system wafer may be present at the same time.

The invention is explained and supplemented by means of examples with two semiconductor wafers using the drawing.

Fig. 1 is a system wafer 1 which was connected with a cover wafer 2 according to an example of a process, namely as a schematic section along line/plane A-A of Fig. 2.

Fig. 2 is a top view of an arrangement as it is shown in Fig. 1.

Fig. 3 is a variant of a conducting connection between system wafer and cover wafer.

Fig. 3[1] is a further variant of a conducting connection between system wafer and cover wafer analogously to Fig. 3.

As it is shown in Fig. 1, low-melting, structured insulating intermediate glass layers 6, 6a, 6b and the electrically conductive solder 5 on the basis of glass (glass paste) connect the system wafer 1 with the cover wafer 2, a selective contacting of the cover wafer 2 with the

[1] Translator's note: should read "Fig. 4"

system wafer 1 and/or between electrically active structures 3 of both wafers being established at the same time (as a product and/or as a process).

As regards the process, the application and the premelting of both glass solders 6, 5 can be implemented separately and successively. Here, the application and premelting of the first glass solder 6 (as a structured layer) is implemented and, separately and, after a certain time interval has expired, the application and premelting of the second glass solder 5 is implemented.

However, an application that takes place successively and a joint premelting are possible, in particular in the temperature range of 450°C.

A conditioning of the glass pastes in the customary extent and the customary processes in semiconductor technology take place prior to a premelting.

The conducting and non-conducting wafer connections are e.g. formed at the same time in the bonding process. For this, the processing temperatures of both used glasses are in the same range.

Metallic strip conductors 4 which are located on the system wafer 1 and are insulated with respect to the substrate by means of an intermediate insulator 7 can be embedded in the area of the non-conducting glass solder. This makes the low-impedance connection of the structures 3 that are to be protected with the cover 2 possible. At the same time, the structures that must be covered by the cover can be packed in a hermetically tight fashion.

The wafer connection 6, 6a, 6b which is mainly mechanically supporting can be implemented by means of a glass solder. As regards it thermal expansion it adapts very

good to silicon. The electric contact surfaces must be kept small in order to minimize mechanical stresses.

In the top view of Fig. 2 the sectional line A is plotted which, provided with a step results in the sectional view of Fig. 1. The cover 2 as the cover wafer is only shown symbolically, actually removed, in Fig. 2, in order to be able to have a look at the structures located beneath it. The wafer 2 is provided with a checked pattern, is unequivocally allocated to Fig. 1 as regards its marginal areas and covers the structure 3 to be protected, but reveals, at the same time, the hermetic sealing and the mechanical support by the isolator layer (the structured layer 6a, 5b, 6) which is set up in a frame-shaped fashion. The bonding islands and the strip conductors 4 can also be reocognized in this picture outside and below the cover wafer 2.

If SOI wafers 8 (silicon on insulator) are used as system wafers as is shown in Fig. 3, there is the possibility to electrically connect substrate 11 of the SOI wafer by means of the conducting glass solder 5. For this purpose, the active layer 9 of the SOI substrate and the buried oxide 10 must be opened at the corresponding site so that the electrically conducting glass solder 5 can flow into the opening and thus contact the carrier wafer.

In order to connect only one or the desired points of the active semiconductor layer 9, the semiconductor layer 9 is insulated at the perforated walls. An intermediate insulator 7, cf. Fig. 1, is not shown in Fig. 3. Since the current SOI-based technologies include these partial steps, there is no extra expenditure.

In a variant to Fig. 3, which was already described there implicitly, but which is completely shown in Fig. 4, the intermediate insulator 7a is defined as regards its area within the opening occupied by the conducting glass solder 5, which, however, does not penetrate up to the semiconductor layer 9 so that it contacts it, since an in particular cylindrical insulator layer 7a is provided which, resting on the top of the semiconductor layer 9, may

still have a circumferential edge in a round, cornered or differently shaped fashion. The strip conductor 4 is only provided above this edge and the semiconductor layer 9. Moreover, the design according to Fig. 4 is designed in the same way as that in Fig. 3 so that reference is made to the description thereof.

If the corresponding electric contact areas and the necessary wafer connection frames are taken into consideration in the design of system wafer 1 and cover wafer 2, the following process for producing the electrically conducting and insulating wafer connections is e.g. possible:

- screen printing for applying the electrically non-conducting glass paste 6 on the cover wafer 2;
- conditioning and premelting of the electrically non-conducting glass paste 6;
- screen printing for applying the electrically conducting glass paste 5 on the cover wafer,
- conditioning and premelting of the electrically conducting glass paste;
- aligning of system and cover wafers;
- bonding under mechanical pressure at the processing temperature of the glasses and/or glass pastes 5, 6.

Alternatively the application of the glasses and/or glass pastes may also be carried out in the reverse order and/or on the system wafer 1 with correspondingly adapted further process steps as shown above.

List of reference numerals

1 System wafer with microelectromechanical and/or electronic structures 3

2 Cover wafer, in particular also provided with electronic structures

3 Microelectromechanical and/or electronic structures to be protected

4 Metal structures, feed lines and bonding islands (bonding pads)

5 Electrically conductive connecting glass (first glass paste, structured)

6 Electrically insulating connecting glass (second glass paste, structured)

7 Intermediate insulating layer

8 SOI wafer (silicon on insulator)

9 Silicon layer (active layer) supporting active electronic structures

7a Insulation in the opening of the active layer

10 Buried oxide of the SOI wafer

11 Supporting wafer (substrate)

12 Insulating ducts in the active layer 9

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